What is claimed is:

1. A method of defining the relative locations of chips on a semiconductor substrate for use in aligning the chips with semiconductor processing or test equipment, comprising:

mounting the semiconductor substrate on a stage of a semiconductor alignment apparatus;

performing a chip alignment comprising obtaining reference coordinates of the central chip on the substrate, and determining whether the substrate is acceptably centered on the stage on the basis of the reference coordinates;

subsequently performing a semiconductor substrate alignment in which data of the relative state of alignment between the substrate and the alignment apparatus is produced, said semiconductor substrate alignment comprising

locating at least two tempates in the central chip with a checker of the semiconductor alignment apparatus, each of the templates comprising a pattern discernible by an imaging device of the checker, capturing the images of the at least two templates with the imaging device, and storing the images and reference coordinates of the at least two templates, and

deriving coordinates of the chips relative to the semiconductor alignment apparatus.

2. The method according to claim 1, wherein the chip alignment comprises

sequentially juxtaposing an alignment ruler of the checker with respective keys disposed around the central chip on the semiconductor substrate, and

determining whether values derived from the juxtaposing of the alignment ruler and the respective keys fall within a permissable range.

3. The method according to claim 1, wherein the semiconductor substrate alignment comprises

using the checker to obtain reference coordinates of a chip adjacent to the central chip, comparing the coordinates of the central chip and the adjacent chip to obtain a correction value that represents a deviation of the substrate in rotational direction or lateral/ longitudinal directions, and adding the correction value to the reference coordinates of the adjacent chip,

moving the semiconductor substrate longitudinally/laterally relative to the checker to obtain reference coordinates of chips located in the peripheral region of the semiconductor substrate, and

adding the correction value to the respective refernce coordinates of the chips located in the peripheral region of the semiconductor substrate.

4. The method according to claim 1, wherein only the image of the at least two templates is captured and stored before the coordinates of the chips relative to the semiconductor alignment apparatus are derived.

5. The method according to claim 1, wherein the images of the at least two templates are captured and stored before the coordinates of the chips relative to the semiconductor alignment apparatus are derived.

6. The method according to claim 1, wherein the respective templates are used to produce the data of the relative state of alignment between the substrate and the alignment apparatus .